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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	:	
John U. KNICKERBOCKER, et al.	:	
Serial No.: 09/817,843	:	Art Unit: 2826
Filed: March 26, 2001	:	Examiner: L. Andujar
For: METHOD AND STRUCTURE FOR AN ORGANIC PACKAGE WITH IMPROVED BGA LIFE	:	Atty Docket: END920000008US1

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Primary Examiner's final rejection of claims 1-3, 17-21, and 35-37.

This brief is in furtherance of the Notice of Appeal, filed in this case on July 6, 2004.

A deposit account authorization has been separately provided in the accompanying FEE TRANSMITTAL.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192.

I. Real Party in Interest

The real party in interest is International Business Machines Corporation.

II. Related Appeals and Interferences

There are no other appeals or interferences known to Appellant, Appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's Decision in this Appeal.

III. Status of Claims

Claims 1-3, 17-21, and 35-37 are pending in the application.

Claims 1-3, 17-21, and 35-37 were rejected and are the subject of this appeal.

IV. Status of Amendments

No amendments were made subsequent to the final rejection.

V. Summary of Invention

Recently, a ball grid array (BGA) package has been disclosed in U.S. Pat. No. 5,148,265, which has ball-like connection terminals over the entire packaging surface of a carrier substrate electrically connected to a semiconductor chip by gold wire bonding. In a BGA package the terminals to be connected to the packaging substrate are formed into ball-like shapes and are

arrayed over substantially the entire packaging surface without deforming the leads as the case for the QFP. Therefore the pitch between the terminals become larger, thereby making surface packaging easier. Furthermore, because the connection terminals are shorter than in a QFP package, the inductance component becomes smaller and thereby the signal transmission speed becomes greater. The resulting BGA package is therefore amenable to high speed processing.[1]

A conventional BGA package base includes a substrate made of an electrically insulating material such as alumina ceramic and a number of connection terminals or bumps formed on the main surface of the substrate. Each connection terminal includes a solder ball bonded to a bonding pad by way of a mass of solder. The bonding pad is formed on a main surface of a substrate treated by a predetermined plating process. The mass of solder typically consists of Pb--Sn eutectic solder or a similar, low melting point solder. The solder ball, itself, is made of a relatively high melting point solder, typically containing a high percentage of lead (Pb), as for example Pb90-Sn10. The solder ball is bonded to the plated surface of the bonding pad by means of the solder mass, thereby constituting a connection terminal. In use, the wired board is mounted on a printed board having bonding pads corresponding in arrangement to those of the wired board in such a manner that their connection terminals are respectively aligned with each other, and then the respective terminals are bonded, electrically connecting the wire board to the printed board.[2]

In the prior art BGA packages, an elastic body is inserted between a semiconductor chip and terminals of a packaging substrate for relieving thermal stress produced due to a difference in thermal expansion between the laminate package substrate and the semiconductor chip. Semiconductor devices having such structures still have problems because of the thermal mismatch. There is much in the literature about the effect of thermal stressing on BGA life. The thermal stresses, attendant to multiple power on/off cycles, literally tear the pads off the package causing loss of electrical connection

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[1] U.S. Patent Application Publication 2002/0137256, paragraph [0004]. This Pre-Grant publication corresponds to the present application.

[2] U.S. Patent Application Publication 2002/0137256, paragraph [0005].

and failure. The industry is trying to overcome this by increasing the pad adhesion to the substrate surface. In contradistinction to current industry practice, *the present invention solves the problem of thermal stress-induced failure by decreasing the adhesion to the laminate.*[3]

FIG. 1 illustrates a conventional fabrication technique. Substrate 100 is shown with a copper foil having a smooth surface 103 and a rough, dendritic surface 105 bonded to a dielectric 107. It is understood that dielectric 107 can be the dielectric of a single or multilayer substrate. The surface of dielectric 107 is imparted with a rough texture through lamination with the dendritic side of the external copper foil. Turning to FIG. 2 conventional subtractive circuitization is illustrated. A negative acting photoresist 209 is applied to the upper surface of copper foil 203. After development, openings 211 are formed in the resist. FIG. 3 illustrates the prior art BGA pad after etching and stripping of the resist. BGA pad 309 is shown anchored to dielectric 307 by the dendritic copper surface 305. It is understood that substantially the entire surface topography of dielectric substrate 300 is dominated by a "replica" of the dendritic surface. *The dendritic topography provides enhanced adhesion.* During thermal stressing of the laminate, such as power on/off cycling, the BGA pads remain `anchored` to the laminate surface through this dendritic structure. As the laminate surface expands and contracts with the thermal excursions the BGA pad moves with the surface. This can place excessive stress on the package. The solder ball anchors the pad to the chip. As the BGA pad moves with the laminate, the stress can fracture the solder connection causing failure. *Accordingly, it would be desirable to provide enhanced BGA life. The present invention achieves this goal by reducing the adhesion of the BGA pad to the laminate.*[4]

Turning now to FIG. 4, *the present invention comprises a BGA package having decreased adhesion of the BGA pad to the laminate surface.* In a first embodiment, the upper surface 401 of dielectric substrate 400 is laminated with external copper foil 407

[3] U.S. Patent Application Publication 2002/0137256, paragraph [0006] (present emphasis).
[4] U.S. Patent Application Publication 2002/0137256, paragraph [0007] (present emphasis).

but in contrast with the prior art, the present invention contacts the less adhesive, shiny side 409 of the foil with the laminate surface 405.[5]

According to [an] aspect of the present invention, an electrically-conductive, "springboard" means is interposed between the BGA pad and the laminate surface. The springboard facilitates electrical conduction while permitting the BGA pad to move independently of the laminate surface in response to thermal cycling.[6]

According to an aspect of the invention the springboard means comprise: a semiconductor substrate; a first compliant dielectric layer formed over said substrate and having at least one first opening formed therein; a first BGA pad formed in said first opening and in electrical contact with said substrate; a second compliant dielectric layer formed over said first compliant layer and having at least one second opening formed therein wherein said second opening is substantially offset from said first opening; a second BGA pad formed in said second opening and in electrical contact with said first BGA pad; a soldermask layer formed over said second compliant layer and having a third opening therethrough in communication with said second BGA pad; a solder ball solderably connected to said second BGA pad and extending through said third opening.[7]

VI. Issues

Claims 1-3 and 17-21 were rejected under 35 U.S.C. § 102(e) over Elenius (6,441,487). The issue on appeal is whether the Examiner has established that the cited art fairly teaches each recitation of the present invention.

Claims 35-37 were rejected under 35 U.S.C. § 102(e) over Elenius (6,441,487) in view of Gotoh (6,204,454). The issue on appeal is whether the Examiner has established that the cited art fairly renders obvious each recitation of the present invention.

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[5] U.S. Patent Application Publication 2002/0137256, paragraph [0021] (present emphasis).
[6] U.S. Patent Application Publication 2002/0137256, paragraph [0009].
[7] U.S. Patent Application Publication 2002/0137256, paragraph [0010].

VII. Grouping of Claims

Claims 1-3, 17-21, and 35-37 stand or fall together as a group.

VIII. Appellant's Arguments

The Examiner has rejected Claims 1-3 and 17-21 under 35 U.S.C. § 102(e) as anticipated by Elenius (6,441,487). The present invention discloses and recites limitations that are neither disclosed, recited, nor anticipated by the cited reference under 35 U.S.C. § 102(e).

The Applicants submit that the threshold issue is whether the Examiner has carried the legal burden to establish a *prima facie* case of anticipation against the present invention. Applicants note that anticipation requires the disclosure, in a prior art reference, of each and every recitation as set forth in the claims.[8] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.[9] To properly anticipate a claim, the reference must teach every element of the claim.[10] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[11] "The identical invention must be shown in as complete detail as is contained in the ...claim."[12] In determining anticipation, no claim limitation may be ignored.[13]

A. Elenius fails to anticipate the present invention because Elenius is silent as to a conductive foil having a smooth side.

Claim 1 recites, in pertinent part: "a conductive foil laminated to said major surface wherein said foil has at least one side having a smooth portion thereof." Elenius is silent as to a conductive foil wherein "said foil has at least one side having a smooth portion thereof." The Examiner explicitly acknowledges the failure of Elenius to teach a smooth surfaced foil. In the

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[8] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[9] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[10] *See* MPEP § 2131.
[11] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[12] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[13] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

Final Office Action, mailed May 5, 2004, in the context of making a rejection under § 103, the Examiner states: "However, Elenius does not disclose the specific roughness of the conductive surface."[14] Not only does Elenius fail to disclose a specific roughness of the conductive foil; indeed, Elenius fails to disclose that one side of the foil must be smooth.

B. Elenius fails to anticipate the present invention because Elenius does not laminate a conductive foil to a substrate.

Regarding claim 1, the Examiner cites Elenius figures 1 and 2 as showing an electronic package comprising a dielectric substrate 22 having a major surface (top surface) and a conductive foil 30 having a smooth portion laminated to the dielectric substrate 22 major surface.[15]

Applicants traverse on the ground that element 22 in Elenius is not a "substrate." Instead, element 22 of Elenius is a "wafer passivation layer."16 The wafer passivation layer is described as "applied over the front surface of semiconductor wafer 14."17 These elements are shown in figure 2 of Elenius. The wafer passivation layer 22 therefore cannot correspond to the "dielectric substrate" recited in claim 1. In the Final Office Action of 04/24/03, the Examiner defines insulating layer 22 as a "substrate" and relies for support on the American Heritage Dictionary. The cited dictionary may be relevant for "general definitions and usages."18 However, the Examiner has used an inappropriate dictionary to provide a definition of "substrate" because "technical dictionaries" provide "specialized meanings as used in particular fields of art."19 International SEMATECH,20 of which the present assignee is a member, provides "specialized," industry standard definitions relevant to the art of the present invention. A "substrate" for the

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[14] Final Office Action, mailed May 5, 2004, page 5, point 14.
[15] *See* Final Office Action, mailed May 5, 2004, page 2, point 4.
[16] *See* lines 20-22 of column 6 of Elenius.
[17] *Id.*
[18] *Inverness Medical Switzerland v. Warner Lambert Co.*, 309 F.3d 1373, 1378 (Fed. Cir. 2002).
[19] *Id.*
[20] ISMT began in 1987 as SEMATECH (Semiconductor Manufacturing Technology), a consortium of U.S. chipmakers that was formed, in partnership with the U.S. government, to help restore American leadership in semiconductor manufacturing. After fulfilling its original mission in the mid-1990s, the consortium withdrew from federal funding and broadened its scope to tackle advanced technology challenges identified in the ITRS. With the addition of new offshore members, the consortium evolved into International SEMATECH in 2000. (*See* www.sematech.org).

instant art is a wafer.[21] Elenius provides "a wafer passivation layer 22 applied over the front surface of semiconductor wafer 14." In view of the industry standard definition, it is improper for the Examiner to define passivation layer 22 as the substrate. Passivation layer 22, therefore cannot correspond to the "dielectric substrate" recited in claim 1. Applicants note that the originally-filed specification provided a definition of "substrate" that is consistent with the industry-standard definition provided by SEMATECH. Discussing a conventional BGA package, the specification taught that the:

> package base includes a substrate made of an electrically insulating material such as alumina ceramic and a number of connection terminals or bumps formed on a main surface of the substrate. Each connection terminal includes a solder ball bonded to a bonding pad by way of a mass of solder. The bonding pad is formed on a main surface of a substrate by a predetermined plating process.[22]

The Examiner equates the redistribution trace 30 of Elenius with the "conductive foil" recited in claim 1. Claim 1 requires that the conductive foil be "laminated to said major surface" of the substrate. By contrast, Elenius' redistribution trace 30 is formed over the wafer passivation layer 22, and is not laminated to a major surface of the wafer 14. The invention recited in claim 1 therefore differs from Elenius, and the rejection is improper.[23]

The Examiner has rejected Claims 35-37 under 35 U.S.C. § 103(a) as rendered obvious by Elenius (6,441,487) in view of Gotoh (6,204,454). The present invention discloses and recites limitations that are neither disclosed, recited, nor rendered obvious by the combination of references cited under 35 U.S.C. § 103(a).

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art

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[21] Substrate. n. *in the manufacture of semiconductors,* a wafer that is the basis for subsequent processing operations in the fabrication of semiconductor devices or circuits. [ASTM F1241]. SEMATECH Dictionary: http://www.sematech.org/resources/publishing/dictionary/index.htm.

[22] U.S. Patent Application Publication 2002/0137256, paragraph [0009].

[23] *See Scripps Clinic and Research Foundation*, 18 USPQ2d 1001.

reference must teach or suggest all the claim limitations.[24] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[25]

C. Elenius and Gotoh, severally and in combination, fail to render obvious the present invention because each of Elenius and Gotoh is silent as to a conductive foil having a smooth side. Elenius and Gotoh, severally and in combination, fail to teach each each recitation of the present invention.

The Examiner states explicitly that Elenius is silent as to a foil having a smooth side.[26] The Examiner cites Gotoh as teaching roughening a foil to provide surface roughness in specified ranges.[27] However, Gotoh does not complete the teaching of Elenius because Gotoh does not teach a smooth side.

D. Because Gotoh teaches away from the present invention, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.

The Examiner acknowledges that Elenius is silent regarding the surface roughness of the foil. The Examiner cites Gotoh as teaching surface roughness. However, the cited art fail to provide incentive for the proposed combination. As the Examiner acknowledges, Gotoh relates to methods to increase the stability of an electrical connection.[28] However, the present invention is directed at a means of decreasing the

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[24] *See* MPEP §2143.
[25] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.
[26] Final Office Action mailed May 5, 2004, page 5, point 14. ("However, Elenius does not disclose the specific roughness of the conductive surface.").
[27] Final Office Action mailed May 5, 2004, page 5, point 14. ("Gotoh discloses a conductive foil having a roughness in a range of 0.3 to 0.5 microns.").
[28] 6,204,454, Col.5, lines 26-33. ("The chemical surface-roughening gives a larger surface roughening than the above physical surface-roughening, ...and that the strength of bonding to the resin is improved in uniformity.") (My emphasis).

stability of a connection.[29] Gotoh specifically teaches away from the present invention. "Teaching away" from the invention is a *per se* demonstration of nonobviousness.[30]

E. Because Gotoh teaches away from the present invention, a person of skill would have no expectation that the combination of Elenius and Gotoh would successfully achieve the present invention.

The legal standard for the *prima facie* case of obviousness requires that the cited art provide a reasonable expectation of success.[31] Gotoh relates to methods of roughening a conductive foil[32] and to the enhanced adhesiveness that such surface roughening provides.[33] A person of skill would not look to the teachings of roughening foil to determine the properties of smooth foil. Gotoh fails to provide a reasonable expectation of success because Gotoh teaches away from the present invention.[34]

The mere fact that prior art may be modified in the manner suggested by the Examiner does not make this modification obvious, unless the prior art suggests the desirability of the modification. No such suggestion appears in the prior art in this matter. The Examiner's attention is kindly directed to *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984), *In re Laskowski*, 10 USPQ2d 1397 (Fed. Cir. 1989) and *In re Fritch*, 23 USPQ2d 1780 (Fed. Cir. 1992).

Concerning the above rejection of the claims, the Examiner should be mindful of the following cautionary statement made by the Court in *Grain Processing Corp. v. American Maize-Products Corp.*, 5 USPQ2d 1788 (Fed. Cir. 1988):

> Care must be taken to avoid hindsight reconstruction by using the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the same result of the claims in suit.

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[29] Claim 1 recites: "An electronic package having selectively controlled contact pad - laminate surface adhesion." The controlled pad-laminate surface adhesion is defined in the specification as decreasing the adhesion. ("The present invention achieves this goal by reducing the adhesion of the BGA pad to the laminate." (Paragraph [0007]).

[30] *U.S. v. Adams*, 338 U.S.39, 148 U.S.P.Q. 479 (1966).

[31] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.

[32] 6,204,454, column 3.

[33] 6,204,454, column 5.

[34] Teaching away from the invention is a *per se* demonstration of nonobviousness. *U.S. v. Adams*, 338 U.S.39, 148 U.S.P.Q. 479 (1966). *A fortiori*, the reference can neither anticipate nor make obvious the present invention.

Likewise, as stated by the court in *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985):

> It is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claim as a blueprint. When prior art references require selected combination to render obvious a subsequent invention, there must be some reason for the combination, other than the hindsight obtained from the invention itself. It is critical to understand the particular results achieved by the new combination.

In the present situation, no such reasoning for the combination exists in the prior art, and nothing in the prior art would suggest the properties achieved by the present invention. Also, see *In re Fine*, 5 USPQ2d 1596 (Fed. Cir. 1988) wherein the Court stated that "one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." Moreover, it is important to keep in mind that statements in the prior art should not be read out of context when evaluating obviousness. See *In re Wright*, 9 USPQ2d 1649 (Fed. Cir. 1989).

The prior art lacks the necessary direction or incentive to those of ordinary skill in the art to render a rejection under 35 USC 103 sustainable. The prior art fails to provide the degree of predictability of success of achieving the properties attained by the present invention needed to have a rejection under 35 U.S.C. 103 sustained. See *In re Mercier*, 187 USPQ 774 (CCPA 1975) and *In re Naylor*, 152 USPQ 106 (CCPA 1966).

Moreover, the properties of the subject matter and improvements which are inherent in the claimed subject matter and disclosed in the specification are to be considered when evaluating the question of obviousness under 35 USC § 103. See *Gillette Co. v. S.C. Johnson & Son, Inc.*, 16 USPQ2d 1923 (Fed. Cir. 1990), *In re Antonie*, 195 USPQ 6 (CCPA 1977), *In re Estes*, 164 USPQ 519 (CCPA 1970), and *In re Papesch*, 137 USPQ 43 (CCPA 1963).

No property can be ignored in determining patentability and comparing the claimed invention to the prior art. Along these lines, see *In re Papesch*, supra, *In re Burt et al.*, 148 USPQ 548 (CCPA 1966), *In re Ward*, 141 USPQ 227 (CCPA 1964), and *In re Cescon*, 177 USPQ 264 (CCPA 1973).

F. Conclusion.

The above discussion renders it abundantly clear that the Primary Examiner erred in finally rejecting claims 1-3, 17-21 and 35-37. Therefore, the undersigned respectfully requests the Board to reverse the Examiner and grant claims 1-3, 17-21 and 35-37.

Respectfully submitted,

By_____

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(First day following Monday, September 06, 2004, Labor Day Federal Holiday)

APPENDIX A
CLAIMS ON APPEAL

1. (Previously presented) An electronic package having selectively controlled contact pad - laminate surface adhesion comprising:

a dielectric packaging substrate having a major surface;

a conductive foil laminated to said major surface wherein said foil has at least one side having a smooth portion thereof, and wherein said smooth portion contacts said major surface of said dielectric packaging substrate.

2. (Original) An electronic package having selectively controlled contact pad - laminate surface adhesion, according to claim 1, wherein said conductive foil comprises any conductive material selected from the group consisting of copper, aluminum, gold, silver, nickel, and chrome.

3. (Original) An electronic package having selectively controlled contact pad - laminate surface adhesion, according to claim 1, wherein said conductive foil comprises any material having high electrical conductivity.

4-16. (Cancelled).

17. (Previously presented) A springboard contact pad – laminate surface contact structure comprising:

a semiconductor packaging substrate having a major surface;

a first mechanically compliant dielectric layer formed over said major surface of said substrate and having at least one first opening formed therethrough;

a first electrical contact pad formed in said first opening and in electrical contact with said substrate;

a second mechanically compliant dielectric layer formed over said first compliant layer and having at least one second opening formed therethrough wherein said second opening is substantially offset from said first opening;

a second electrical contact pad formed in said second opening and extending over a portion of said first electrical contact pad and contacting said first electrical contact pad;

a mask layer formed over said second compliant layer and having a third opening therethrough in communication with said second electrical contact pad; and

a solder ball solderably connected to said second electrical contact pad and extending through said third opening.

18. (Original). A springboard contact pad - laminate surface contact structure, according to claim 17, wherein said mask layer is a soldermask.

19. (Original). A springboard contact pad - laminate surface contact structure, according to claim 17, wherein said mechanically compliant layers comprises dielectric materials selected from the group consisting of photoresist, photoimageable dielectrics and prepreg.

20. (Original). A springboard contact pad - laminate surface contact structure, according to claim 17, wherein said electrical contact pads comprise highly conductive material selected from the group consisting of copper, copper foil, plated copper foil, and other suitable materials.

21. (Original). A springboard contact pad - laminate surface contact structure, according to claim 17, wherein said electrical contact pads comprise highly conductive material selected from the group consisting of aluminum, gold, silver, nickel, and chrome.

22-34 (Cancelled).

35. (Previously presented) An electronic package having selectively controlled contact pad – laminate surface adhesion, according to claim 1, wherein the smooth portion of the conductive foil has a surface roughness less than about 2.0 micron.

36. (Previously presented) An electronic package having selectively controlled contact pad – laminate surface adhesion, according to claim 35, wherein the smooth portion of the conductive foil has a surface roughness less than about 1.0 micron.

37. (Previously presented) An electronic package having selectively controlled contact pad – laminate surface adhesion, according to claim 36, wherein the smooth portion of the conductive foil has a surface roughness less than about 0.01 micron.

Appendix B

Cited Reference

Technical Reports and Publishing Resources

DICTIONARY OF SEMICONDUCTOR TERMS

A-Am | An-Az | B | C-Ch | Ci-Com | Con-Cz | D-De | Df-Dz | E-En | E
Fm-Fz | G | H | I | J-K | L | M-Mes | Met-Mz | N | O | P-Ph | Pi-Pq | Pı
S-Se | Sh-So | Sp-Sta | Ste-Sz | T-Th | Ti-Tz | U-V | W-Z

"Ste-Sz"

steam atmosphere
n
the atmosphere in a heated, closed vessel containin sufficient venting so that a temperature of 100 degr degrees C is maintained at one (1) standard atmosp atmosphere is used to accelerate surface aging char during lead solderability testing. [SEMI G35-87]

steam bath
n
exposure to flowing steam or to another source of h temperature of flowing steam, at one atmosphere p [Adapted from SEMI C1-94]

step
n
1 : a single action in the performance of an operatic process. [SEMATECH] 2 : the transitions from lower wafer pattern to upper layers; the topography of a p [SEMATECH]

step and repeat
n
an operation that, by the use of a stepper, repeats t the wafer as the stage makes small steps in the X a operation dimensionally positions multiples of the sa intermixed functional patterns on a given area of a p film by repetitions, contact printing, or projection pr single original pattern of each type. [SEMATECH]

step coverage
n
the ratio of thickness of film along the walls of a ste thickness of the film at the bottom of a step. Good s reduces electromigration and high-resistance pathw [SEMATECH]

step function transient response *n* — *in regulator performance testing*, a plot of outlet pre time when switching between two flow rates. [SEMA

step response time *n* — *in mass flow controller testing,* the time between th change and the moment the actual flow first enters band. [SEMI E17-91]

step stress test *n* — a test that consists of several stress levels applied s periods of equal duration to a sample. During each stress level is applied, and the stress level is increas step to the next. (Copyright 1993 IEEE. All rights re

stepper *n* — equipment used to transfer a reticle pattern onto a [SEMATECH]

STM — see scanning tunneling microscope.

stoichiometric *adj* — describes a quantitative relationship, usually expres between two or more chemical substances undergoi chemical change; the point at which the chemical re stabilizes. [SEMATECH]

storage temperature limits *n* — *in a mass flow controller,* the temperature limits to may be subjected in an unpowered condition. No pe impairment will occur, but minor adjustments may restore performance to normal. [SEMI E18-91]

streak *n* — *in the surface roughness measurement of flat panel substrates,* a defect whose appearance is a transpa glass substrate surface. A streak can be caused by microsurface discontinuity or a cord, due to the hete glass composition. [SEMI D9-94]

stream *n* — *in SECS communication*, a category of messages int support similar or related activities. NOTE-A specific specific activity within a stream is called a function.

street — see scribe line.

stress marks — thin, radial lines that start in the center of a photopl

n outward. The lines are colored. [SEMI P3-90]

stress test
n exposure of components to extreme mechanical, ter humidity, and biased conditions. [SEMATECH]

striation
n 1 : a helical feature on the surface of a silicon wafer local variations in impurity concentration. [ASTM F1 resist coat caused by separation of the chemical cor resist. [SEMATECH]

stripper
n a chemical solvent used to remove resist film from \ [SEMATECH]

stripping
n an operation that completely removes a resist coati

stripping solution
n a chemical mixture that will remove either processe unprocessed resist from its substrate. [ASTM F127-

stuck-at fault
n a fault in a manufactured circuit causing an electrica stuck at a logical value of 1 or a logic value of 0, inc input to the circuit. [1994 National Technology Roac Semiconductors]

stylus method surface roughness measuring instrument
n *in the roughness measurement of flat panel display surfaces,* an instrument that traces on a section of a stylus, records irregularity on the surface in an enla indicates irregularity amplitude as roughness param D7-94]

subdiffused layer see buried layer.

sub-fab
n the area located underneath the processing floor of contains support equipment (pumps, etc.) for proce [SEMATECH]

subject
v to expose to or apply. [SEMI F12-93]

submersion *in fluid distribution systems*, a transparent containe

container *n*
low surface tension fluid at 23 ±3 degrees C, used f leakage. [SEMATECH] Also called *submersion tank*.

submersion tank
see submersion container.

submicrometer process *n*
a sequence of steps that produces integrated circuit widths (critical dimensions) of less than 1 micromet

submittals *n*
technical data about a specific product or system; a allows contractors to verify the design intent prior t construction. [SEMATECH]

substrate *n*
in the manufacture of semiconductors, a wafer that subsequent processing operations in the fabrication semiconductor devices or circuits. [ASTM F1241]

subsystem *n*
an assembly of two or more components that is ma single entity. A subsystem must be combined with c additional components or subsystems to form a com [SEMI F1-90]

sulfur hexafluoride (SF6) *n*
a colorless and odorless gas that has a low toxicity. hexafluoride is used as a plasma etchant and as an chemical vapor deposition. [SEMI C3.24-90] Also se etch.

sulfuric acid (H2SO4) *n*
a strong, poisonous, corrosive liquid that will mix wi that will dissolve most metals. Sulfuric acid is used and to remove resist. [SEMI C1.16-90]

supplier-dependent uptime *n*
the percentage of time that the equipment is in a cc perform its intended function during the period of o minus the sum of user maintenance delay, out-of-s downtime, and facilities related downtime. This calc only user maintenance delay from the period, there account supplier delays for parts and service. [SEMI see equipment states.

supply pressure effect *n*
in determining regulator performance characteristic an inlet pressure change on the outlet pressure of a [SEMATECH]

support tool *n* — a mechanical device that, although not a part of a p equipment, is required by it and becomes integral w course of normal operation. Examples include wafer and probe cards. [SEMI E10-92]

surface *n* — 1 : the boundary that separates an object from anot substance, or space. [ASME B46.1-85] 2 : *in electrc for chemical analysis (ESCA)*, that volume from whi photoelectrons can escape. [SEMATECH]

surface area index *n* — *in determining surface roughness by contact profilo scanning tunneling microscopy*, the area of a best fi surface) subtracted from the actual area calculated divided by the ideal area, and multiplied by 1,000. [

surface chip — see peripheral chip.

surface contamination *n* — *in flat panel display substrates*, an area that is cont organic or inorganic material. [SEMI D9-94]

surface defects *n* — 1 : *in the manufacture of silicon on sapphire (SOS) wafers,* mechanical imperfections, SiO2 residual dus imperfections visible on the wafer surface. Some ex surface defects are: dimples, pits, particulates, spot smears, hillocks, and polycrystalline regions. [SEMI *flat panel display substrates*, a marking, tearing or s abrasion on the glass surface. [SEMI D9-94]

surface imaging *n* — multilayer resists on which the image to be transfer onto a thin resist layer on the surface when develop layer serves as a mask to pattern a thick resist laye employed for forming the image on the wafer. [199 Technology Roadmap for Semiconductors]

surface micro defect — see crystal originated particle.

surface profile *n* — the contour of the surface in a plane perpendicular t unless some other angle is specified. [ASME B46.1-

surface protrusions or intrusions *n*
in the manufacture of molded plastic packages, plas (such as bumps or blisters) or recesses (such as pit: any surface of the package. [SEMI G54-93]

surface roughness *n*
the finer irregularities of the surface texture, usuall irregularities that result from the inherent action of process. Examples include traverse feed marks and irregularities within the limits of the roughness sam [ASME B46.1-85]

surface texture *n*
the topographic deviations of a real surface from a surface. NOTE-Surface texture includes roughness, lay. [ASTM F1241]

surrogate gas *n*
in the calibration of mass flow devices, a gas intend the calibration characteristics of another gas. [SEMI

surround shape *n*
a geometric configuration around the symbol, which additional safety information. [SEMI S1-90]

swab bud *n*
in determining surface associated biofilm, the portio makes contact with the sample, as distinct from the [SEMATECH]

SWIM *n*
a software system and data infrastructure that allow manufacturing modeling applications and CIM syste integrated in a common framework. A primary capa that it supports the transfer of common data betwe referenced applications and systems. Through its ta SWIM also provides utilities that facilitate modeling Abbreviation for *semiconductor workbench for integ* [SEMATECH]

swirl *n*
helical or concentric features that are visible to the after preferential etch and appear to be discontinuo magnification. [ASTM F1241]

symbol *n*
1 : a graphic representation, either abstract or repr a hazardous situation and/or evasive actions to be t harm. It may include a description of protective equ used to eliminate or reduce the hazard to an accept

[SEMI S1-90] Also see sign. 2 : *in the bar code mar wafers,* a combination of characters, including start/ quiet zones, data characters and check characters, t by a particular symbology and that form a complete entity. [SEMI T1-93]

symmetrical valve *n* — a valve bilaterally identical with respect to its center similar flow and pressure characteristics in either di [SEMATECH]

symptom *n* — a subjective indication of a disease or of a change ir perceived by the person. [SEMATECH]

synthesis design *n* — the automatic or semiautomatic creation or refinem at a given level of abstraction; for example, local sy synthesis, etc. [1994 National Technology Roadmap Semiconductors]

synthesis for testability *n* — the synthesis of logic from a higher level descriptior considerations to ensure that the final design can re [1994 National Technology Roadmap for Semicondu

system *n* — 1 : an integrated whole, composed of diverse, inter specialized structures and subfunctions. [SEMATECH integrated structure of components and subsystems performing, in aggregate, one or more specific funct 90]

system architecture — see architecture.

system bytes *n* — a 4-byte field in a header; used for message identifi E4-91]

system default *n* — *in communications and control of semiconductor ma equipment,* a state or states in the equipment beha that are expected to be active at the end of system and the value or values that specified equipment va expected to contain at the end of system initializatic 94]

systemic effects — describes effects on the metabolism and excretory f

(SYS) *adj* [SEMATECH]

system initialization *n* *in communications and control of semiconductor ma equipment,* the process that an equipment performs system activation, and/or system reset. This proces prepare the equipment to operate properly and acc equipment behavioral models. [SEMI E30-94]

A-Am | An-Az | B | C-Ch | Ci-Com | Con-Cz | D-De | Df-Dz | E-En | E Fm-Fz | G | H | I | J-K | L | M-Mes | Met-Mz | N | O | P-Ph | Pi-Pq | P S-Se | Sh-So | Sp-Sta | Ste-Sz | T-Th | Ti-Tz | U-V | W-Z

Contact: info@sematech.org
Last update: 01/05/04

PTO/SB/17 (10-03)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/817,843-Conf. #9394
Filing Date	March 26, 2001
First Named Inventor	John U. Knickerbocker
Examiner Name	L. Andujar
Art Unit	2826
Attorney Docket No.	20135-00310-US

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 09-0457

Deposit Account Name: International Business Machines Corp.

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		x		=	
Independent Claims		-3** =		x		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY

(Complete *(if applicable)*)

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Signature				Date	September 7, 2004